REMARKS

Claims 1-3, 6, 10-13, 16-24, 26, 28-33 and 35-37 are pending. Claims 1, 6, 10 and 19 are amended. Claims 5, 15 and 28 are cancelled. Claims 4, 7-9, 14, 25, 27 and 34 have been cancelled in a previous amendment.

Applicants acknowledge and thank the Examiner indicating that claims 28-31 contain allowable subject matter, and would be allowed if written in independent form including all the limitation of base claim and any intervening claims. The subject matter of claim 28 has been incorporated into base claim 19. Accordingly, claims 19-24, 26 and 29-31 are in a condition for allowance.

CLAIM REJECTIONS 35 USC 112

Claims 10-13 and 15-18 are rejected under 35 USC 112, second paragraph as being indefinite. Applicants traverse this rejection.

The Examiner alleges that amendments made to claim 10 in response to the last office action makes claim 10 "misleading." Claim 10 is a generic independent claim. The specification and FIGS. disclose several embodiments. With all due respect, Applicants are not clear why the Examiner is of the opinion that claim 10 is "misleading." Applicants request the Examiner to carefully re-read claim 10, specifically the second and third transistors as they apply to the FIGS. If after re-reading claim 10 and the Examiner is still of the opinion that claim 10 is misleading, Applicants respectfully request the Examiner to further clarify his position as to why he is of the opinion that claim 10 is "misleading."

CLAIM REJECTIONS 35 USC 103

Claims 1-3, 5-6, 10-13, 15-18, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over Hardee (US 6,580,306) in view of Amanai (US 6,128,230). Applicants traverse this rejection.

Initially, Applicants would like to remark on the Examiners' combination allegation. The Examiner alleges that "it would have been obvious to one of ordinary skill in the art to supply second MOS transistor 16 [Applicants will assume the Examiner meant transistor 14] of Hardee with a row address signal given in a memory device, and/or to replace Amanai's level shifting type circuit 15 with Hardee's device." In Amanai, reference numeral 15 is a level shift circuit, which is much more complex than a simple transistor of Hardee. In other words, in order for the Examiner's former allegation to be true, an entire level shift circuit of Amanai must replace a transistor of a level shift circuit of Hardee. Applicants submit that it would not make sense to combine two different types of level shift circuits by replacing a transistor of one level shift circuit (Hardee) with cross-coupled transistors (Amanai), thereby creating some hybrid level shift circuit. Therefore, it is more logical to replace "Amanai's level shifting type circuit 15 with Hardee's device."

Applicants have amended independent claims 1 and 10 by incorporating the subject matter of claims 5 and 15, respectively. In rejecting claims 5 and 15, the Examiner rejects the claims by alleging that it would have been obvious to add an inverter to the device of Hardee. Applicants will assume that the Examiner meant to allege that claims 5 and 15 are rejected as being obvious over Hardee in view of Amanai, because the Examiner uses Amanai as showing "the second MOS transistor is controlled by a row address signal in a memory device." Without both Hardee and Amanai, the Examiner's obviousness rejection fails.

Under U.S. Patent Law, if a proposed modification would render a prior art reference unsatisfactory for its intended purpose, then there is no motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); M.P.E.P. § 2143.01(V).

Amanai clearly teaches that a combination of level shift circuits 15 and 16 comprise a row main decoder MD. The level shift circuits 15 and 16 "are complementary to each other." The MD supplies an output signal XB to a sub-decoder SD, and the SD selects a row of memory cell MC. Column 1, lines 11-41. In addition, Amanai specifically discloses on column 1, line 66 to column 2, line 13:

> A first level shift circuit 15 is composed of two pairs of transistors which are connected between a mode switching power supply (VPX) node and a ground node in series. More specifically, the level shift circuit 15 is composed of a p-channel transistor PM1 and an n-channel transistor NM1, and a p-channel transistor PN2 and an n-channel transistor NM2.
>
> **With such a structure**, an output of a NAND gate 13 is given to a gate of the transistor NM1 while an output of an inverter circuit 14 is given to a gate of the transistor NM2. Further, a series connection point between the transistor PM1 and the transistor NM1 is coupled to a gate of the transistor PM2 while a series connection point between the transistor PM2 and the transistor NM2 is coupled to a gate of the transistor PM1. (Emphasis added.)

A can be appreciated from the above remarks and teachings of Amanai, if one or both of the level shift circuits 15 and 16 is replaced with the Hardee's device as alleged by the Examiner, such a modification would destroy at least one intended purpose of Amanai. For example, if only one of the level shift circuits 15 and 16 is replaced with the Hadree's device, then Amanai's purpose of providing complementary level shift circuits 15 and 16 is destroyed. If both of the level shift circuits 15 and 16 are replaced with the Hardee's device, then Amanai's purpose of providing cross linked transistors is destroyed.

In addition and/or in the alternative, the Examiner in allowing the subject matter of claim 28-31, opines "[t]here is presently no strong motivation to modify or combine any prior art reference(s) to ensure the first internal node is coupled to the row decoder and driver block of the memory device, wherein that block selectively drives word lines of the memory device in response to row address signals."

As remarked above, independent claims 1 and 10 are amended. For example, the subject matter of claim 5 and 15 has been incorporated into claims 1 and 10, respectively. Amended claim 1 recites, *inter alia*, "an inverter coupled to a connection node of the first and second transistors, the inverter drives a word line of a memory device." The Examiner will note that original dependent claims 5 and 15 similarly recite the subject matter of allowed claim 28. Applicants submit that if the subject matter of claim 28 is allowable, then for the same reasons, the subject matter of amended claims 1 and 10 are also allowable.

For at least the reasons give above, Applicants submit that the teachings of Hardee cannot be combined with the teachings of Amanai without destroying an intended purpose of Amanai, and/or independent claims 1 and 10 are patentable for the same reasons claim 28 (independent claim 15) is allowable. Dependent claims 2, 3, 6, 10-13, 16-18, 32-33 and 35-37 are also patentable for respectively depending on an allowable base claim.

Claims 1-3, 5-6, 10-13, 15-18, 32-33 and 35-37 stand rejected under 35 USC 103(a) as being unpatentable over Wright in view of Amanai (US 6,128,230). Applicants traverse this rejection.

For at least the same reasons why Amanai cannot be combined with Hardee, Applicants submit that Amanai cannot be combined with Wright, and/or independent claims 1 and 10 are patentable for the same reasons claim 28 (independent claim 15) is allowable. Accordingly, independent claims 1 and 10 are patentable over the Examiner cited references. Dependent claims 2, 3, 6, 10-13, 16-18, 32-33 and 35-37 are also patentable for respectively depending on an allowable base claim.

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CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-3, 5, 6, 10-13, 15-24, 26, 28-33 and 35-37 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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